AN E - MODE GaAs FET OPERATING AS A SINGLE BALANCED GATE MIXER

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ABSTRACT

The objective of this paper is to describe the design details of a semi-monolithic single balanced gate mixer for DBS applications. In order to obtain a low noise figure and high conversion gain it was decided to employ enhancement mode MESFETs, thus avoiding the need for a negative supply. The non-linear modeling is briefly described and contributed to the success of the mixer performance. An SSB noise figure of 6.0 dB was measured from 10.7 to 11.8 GHz with a conversion gain of 7.0 dB +/- 1.0 dB, with only + 3.0 dBm of LO power. The third order intercept point is equal to + 13.0 dBm, adequate for LNB applications.

INTRODUCTION

The evolution of the MMIC technology gives the mixer designer new possibilities to develop new circuit approaches and to improve the traditional ones. In the literature many recent MMIC mixers were reported to present high conversion gain and high linearity. However, when bandwidth and low noise figure are the most important specifications required from a communication system, the single gate mixer is still the preferred circuit topology[1]. The objective of this work is to describe the techniques employed in the design of a semi-monolithic single gate mixer, using Enhancement mode MESFETs as the non-linear elements. Besides the advantage of requiring only positive supply voltage they present higher transconductance and lower noise figure when employed as small signal devices, compared to similar depletion mode transistors[2]. Electrically, the main difference resides in the pinch-off voltage, which is set to 0.1 volts by a suitable choice of the technological parameters.

THE E-FET EQUIVALENT CIRCUIT

It was found that the Statz-Pucel model is capable of representing the large and the small signal operation of positive value and fitting the other parameters according to standard procedures. The DC measurements were done on a test cell measuring 0.5 X 160 μm² and the RF measurements on a larger device, measuring 0.5 X 320 μm². The main DC parameters are a threshold voltage of + 0.12 volts, a maximum drain current of 100.0 mA/mm @ VDS = 3.0 volts and a maximum DC transconductance of 170.0 mS/mm. The key high frequency parameters are an fT of 23 GHz and a minimum noise figure of 1.0 dB at 12 GHz.. The non-linear model for the device is shown in figure 1, where two elements have been added to the conventional topology: a parallel RC network in series with the drain and source; a series RC in parallel with the output conductance. They were added for best model fit to the measured DC and RF parameters.

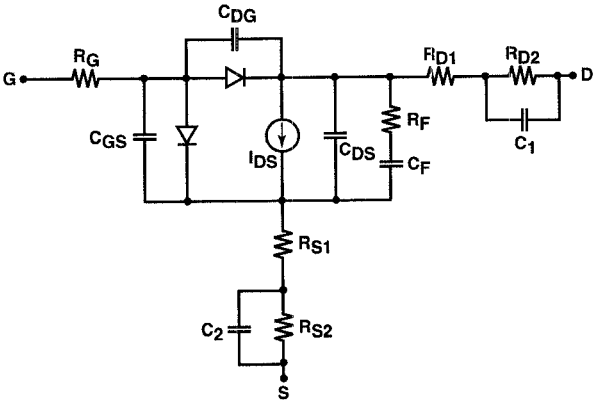

Fig 1. Equivalent Electric Circuit

THE MIXER DESIGN APPROACH

It has already been demonstrated[3] that frequency conversion in MESFETs can be generated by the modulation of the non-linear current source by means of a large LO voltage applied to the gate. In the case of E-mode gate mixers, it is also possible to obtain frequency conversion by modulating the gate-to-source diode. However, this option results in high noise figure, originating from losses introduced by the Schottky diode conduction, and thus should be avoided by limiting the applied LO power. The other input non-linearities such as the gate to source capacitance and input resistance, are not important in the conversion process but will

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affect the matching of the LO and RF signals. All other components from the model are considered linear at the frequencies of interest in the present work.

Efficient frequency conversion is obtained when the device terminations enable the non-linear current source to be fully modulated by the large signal local oscillator voltage, and the RF and IF impedances are properly matched. The design is accomplished by first linearizing the non-linear model for synthesizing the matching networks, and then by simulation of the full mixer circuit for determining its performance. The linearization is obtained by replacing the non-linear elements from the model by fixed equivalent values which are dependent both on LO voltages and Input/Output terminations[4]. The equivalent values are generated from non-linear analysis, by applying to the gate a large signal voltage generator in series with a small signal voltage generator as illustrated in figure 2, and reading the resulting currents. The non-linear simulator employed in this work is the commercial software package, MDS by HP-EESOF.

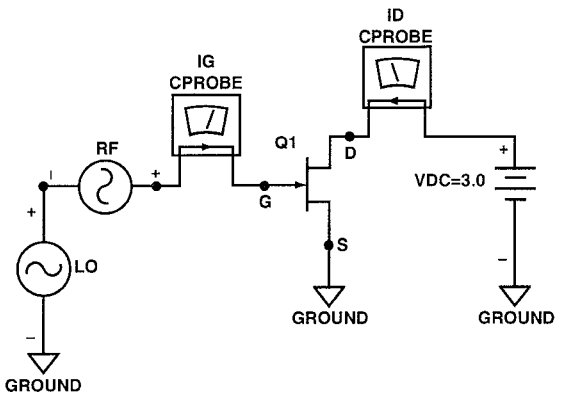

Fig 2. Circuit for simulating the mixer parameters

This topology is similar to the one employed for gate mixers, where a low pass filter is connected to the drain to short all high frequency components except the IF signal and a high pass filter on the gate which shorts the low frequency ones. This procedure reduces the dependency of the linearized parameters to the LO voltage. Making the further assumption that the LO voltage is large enough to drive the device from pinch-off to IDS = Imax, the linearized values can be used to design an initial network to match the mixer to a 50 ohms generator. The full mixer circuit is then submitted to non-linear analysis and new equivalent values are obtained for correcting the initial model and the matching network It was found this process converges with a few iterations.

The equivalent gate-to-source capacitance is obtained by simulating the input impedance as follows:

Zin = IGS(fRF)/VG(fRF) Small signal pumped impedance
ZIN = IGS (fLO)/VG(fLO) Large Signal impedance

The non-linear current source in the model can be replaced by an equivalent transconductance in parallel with an output conductance, which was assumed to be constant and equal to the small signal value. In a gate mixer this element is generally shunted by a low impedance at the LO frequency, so that there is no large voltage swing across its terminals and the small signal assumption can therefore be applied. The equivalent values are obtained by relating the currents and voltages as follows:

GM = IDS(fLO)/VG(fLO) Large Signal transconductance
gmo = IDS(fRF)/VG(fR) Small Signal transconductance
gm1 = IDS(fIF)/VG(fRF) Conversion transconductance

A representation of the various transconductances as a function of voltage is found in figure 3. It is interesting to note that gmo is higher than the large signal value at the point of maximum modulation, where the gate peak voltage is equal to 0.8 volts. However, this is nearly half the maximum DC value which is equal to 50 mS.

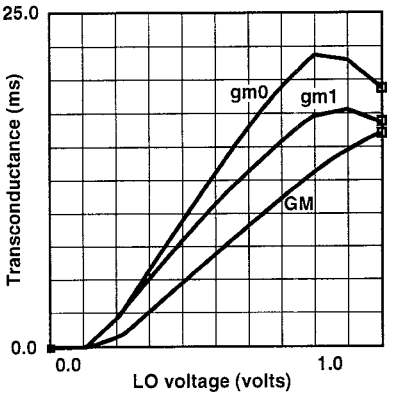

Fig 3. Transconductance components in a mixer

CIRCUIT DESIGN

The mixer was designed for DBS applications, and intended to cover the RF band from 10.7 to 11.8 GHz with a LO frequency of 9.75 GHz. The image frequency is filtered by a bandpass filter and only the upper sideband is converted to IF. The approach to design a gate mixer in MMIC was to split the circuit in elements on-chip and elements off-chip. Thus, the problem of adding the LO and RF before applying them to the gate can be done externally using conventional techniques, and internally only the drain terminations are incorporated. The preferred approach to add the RF and LO signals, was to use two mixers in a balanced configuration, employing a rat race hybrid coupler as a combiner. Applying the RF signal on the balanced ports, all source parasitics are neglected by the 180° phase shifting, ensuring a good performance of the mixer, even when assembled in a highly inductive package.

The single ended mixer design started with the recognition that in MMIC technology, it is not practical to employ large inductors, for the area they require and the excessive loss they I ntroduce. Therefore, it was decided to choose a drain termination that trades off low impedance at RF and LO with a resistive load at IF that gives a reasonable

conversion gain. A rough estimate was made by means of the classical conversion gain equation, CG, and the previously determined equivalent values.

$$CG = \frac{gm1}{4(\omega.Ceq)^2} \cdot \frac{Rd}{Rin}$$

The chosen drain termination consist of a low shunt capacitor and a realizable spiral inductor designed to present an IF impedance of 100 ohms, which gives nearly 7.0 dB conversion gain.

The linearized RF impedance was matched to 50 ohms by means of bonding wires and microstrip lines, taking into account the package parasitics. The bonding wires are the main matching elements and they also provide operation in class B, by DC connecting the gate to ground. The matching elements were determined from optimization techniques on Touchstone, by HP-EESOF. The optimization process requires a control on the voltage across CGS, otherwise a good match can be obtained at RF with a LO peak voltage that is different than the assumed value which invalidate the linearized model. Figure 4 gives a simplified schematic of the single balanced mixer.

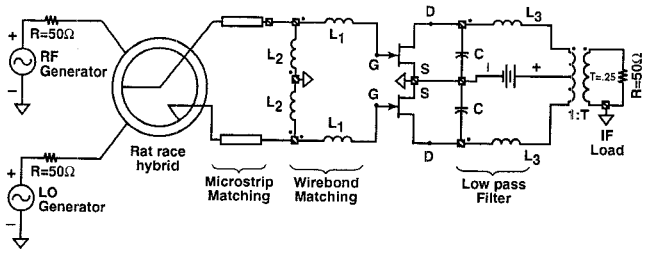

Fig 4. Schematic of the single balanced mixer

The initial simulations carried out for the full mixer revealed an input return loss better than 15 dB for the RF band, and only 3.5 dB for the LO. Thus, this particular matching topology is not able to simultaneously match the RF and LO impedance. However, the calculated LO voltage across CGS is equal to 0.82 volts which validates the initial large voltage assumption. The next set of simulations was aimed to investigate the dependence of conversion gain on LO power at an RF frequency of 11.0 GHz, for an IF load of 100 ohms. The resulting conversion gain increases monotonically with LO power, and peaks when the LO power is + 4.0 dBm, yielding 8.0 dB. Simulation showed a conversion gain of 8.5 dB flat within 0.5 dB over the band of 10.7 to 11.8 GHz. However, this performance cannot be measured directly due to the impedance of the measuring instruments. Therefore, in order to characterize the mixer, the IF load was transformed to 50 ohms by a LC low pass filter. The circuit again simulated with the IF transforming circuit, and the resulting gain is still in the order of 8.0 dB but in-band ripple increased to 2.0 dB.

REALIZATION AND MMIC FABRICATION

The on chip components are the active devices, and the lumped components connected to the drain side of the circuit. The active devices and resistors were fabricated by standard FUJITSU ion implantation process on a 250 μm thick GaAs substrate. The gate geometry for the enhancement mode MESFET is equal to 0.5 x 320 μm^2, the drain to source capacitors are of MIM type and the output inductor is a planar square spiral type. The off chip components comprises the RF and IF matching networks previously described.

The chip was assembled in a low cost ceramic package, featuring low losses and negligible ground inductance. The balanced outputs were connected to an external balun, type ZAPDJ-2 by Mini-Circuits, using semi-rigid cables. A photo of the test fixture is shown in figure 5, which shows a chip resistor on the LO path crossing the ratrace hybrid. This element, besides providing the crossover, improves the LO matching.

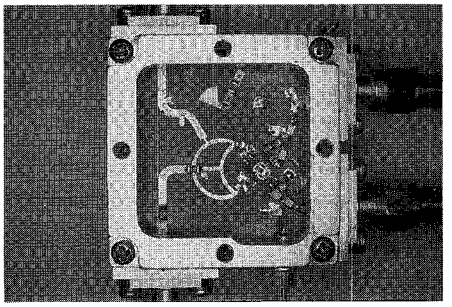

Fig 5. Photo of the mixer test fixture.

EXPERIMENTAL RESULTS

The main purpose of the experimental results has been to verify the viability of the design technique and to investigate the potential of this mixer, for application in MMIC sub-systems. Before taking the measurements, the gate and drain matching elements had to be tuned to compensate effects not completely predicted in the simulations. This included the RF adjustments on soft board to compensate the uncertainty in the bonding wires matching, and the IF adjustments with chip inductors and capacitors to compensate their inherent parasitics.

The first set of measurements refers to frequency response performance. The result of figure 6 shows a noise figure 6.0 dB and a conversion gain ranging from 6.0 to 8.0 dB over the IF band 0.95 to 2.05 GHz at a LO power of + 3.0 dBms. The theoretical response is also shown in the same figure, an is nearly 1 dB higher and 1 dB smoother than the experimental. The amplitude ripples are due to the cables used to connect the IF outputs to the external balun for adding up the signals.

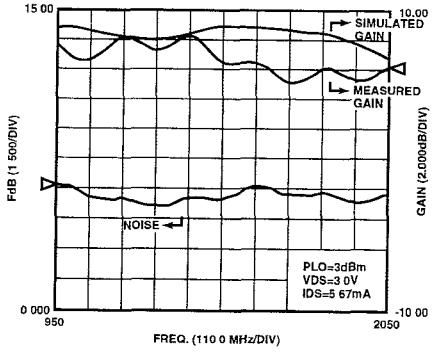

Fig 6. Experimental Conversion gain and noise figure

The measured L to R isolation is 20 dB and the L to I is greater than 45 dB. The LO return loss is equal to 8.0 dB and the RF return loss is better than 10.0 dB. The influence of source match on the mixer performance was determined for VSWRs of 1.1:1, to 3:1 and we found a maximum degradation of 1.5 dB in the noise figure. Another important parameter is the influence of image termination which was measured with a low loss phase shifter in series with the image reject filter. We observed a maximum degradation of 1.0 dB in the noise figure and 1.5 dB on the conversion gain for a 360° phase change.

The second set of measurements are related to power performance, which in this context is expressed by the third order intercept point. The dependence of this parameter on LO power is shown in figure 7. The IP3 increases nearly monotonically with the LO power, peaking at + 15.0 dBm for a LO equal to + 10.0 dBm. The influence of drain bias on the noise figure is very mild, changing only 0.4 dB when VDS change from 1.0 to 4.0 volts. The DC consumption is equal to 5.5 mA when the LO power is set to + 3.0 dBm.

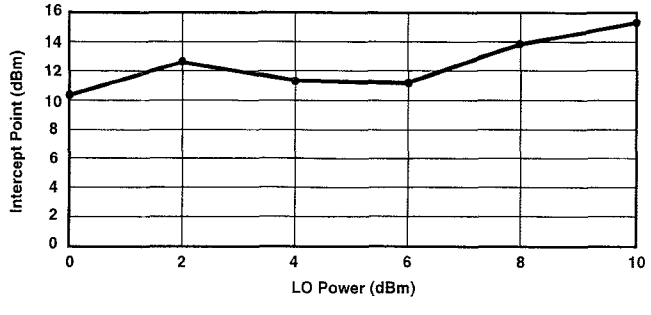

Fig 7. Third Order Intercept point versus LO power

Finally, a test cell has been built with a depletion device which posses the same gate geometry, and allow a comparison between depletion and enhancement devices as mixer elements. The device was biased at VGS = -1.4 volts, VDS = + 3.0 volts, and the LO power was set to + 3.0 dBm. The mixer circuit provided 6.7 dB noise figure and 5.0 dB conversion gain in the same RF band, proving the superiority of enhancement devices over depletion devices for this application.

CONCLUSIONS

The approach herein described to employ commercially available linear and non-linear software to the design of gate mixers proved to be successful. The key to obtain the described performances was to apply enhancement devices, which present low noise figure, high transconductance and does not require negative bias. A prototype circuit was fabricated and evaluated with on-chip and off-chip components. The mixer presented a noise figure lower than 6.0 dB over the 10.7 to 11.8 GHz band and a third order intercept point of + 13.0 dBm, with only + 3.0 dBm LO power. These features makes this component attractive to satellite receivers since fewer LNA stages are required in the front end, and its wide dynamic range guarantees conversion linearity, an important parameter in digital video reception.

ACKNOWLEDGMENTS

The authors would like to thank Hao Dang and Kenji Yoshida for their contribution during assembling and measurements. Thanks are also due to Dr. Yoshio Aoki for his support and encouragement

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